

WHAT IS CLAIMED IS:

1 1. Clock control circuitry for selectively applying a
2 clock signal to a digital processing component, said clock signal
3 capable of being changed to a plurality of operating frequencies,
4 said clock control circuitry operable to (i) receive a command to
5 change a first operating frequency to a second operating
6 frequency, (ii) in response to said command, disable said applied
7 clock signal, (iii) generate a test clock signal having said
8 second operating frequency, (iv) apply said test clock signal to
9 a power supply adjustment circuit, and (v) sense a status signal
10 from said power supply adjustment circuit indicating that a power
11 supply level of said digital processing component has been
12 adjusted to an optimum value suitable for said second operating
13 frequency.

1 2. The clock control circuitry for selectively applying a
2 clock signal to a digital processing component as set forth in
3 Claim 1 wherein said clock control circuitry is further operable
4 in response to said status signal to set said applied clock
5 signal to said second operating frequency.

1 3. The clock control circuitry for selectively applying a
2 clock signal to a digital processing component as set forth in
3 Claim 2 wherein said clock control circuitry is further operable
4 to enable said applied clock signal.

1 4. The clock control circuitry for selectively applying a
2 clock signal to a digital processing component as set forth in
3 Claim 1 further comprising clock divider circuitry and a
4 controller.

1 5. The clock control circuitry for selectively applying a
2 clock signal to a digital processing component as set forth in
3 Claim 4 wherein said controller is operable to disable said
4 applied clock signal in response to said received command and
5 enable said applied clock signal in response to said status
6 signal.

1 6. The clock control circuitry for selectively applying a
2 clock signal to a digital processing component as set forth in
3 Claim 4 wherein said clock divider circuitry is operable to
4 generate said test clock signal having said second operating
5 frequency.

1 7. The clock control circuitry for selectively applying a
2 clock signal to a digital processing component as set forth in
3 Claim 1 further operable to set said applied clock signal to said
4 second operating frequency as a function of said test clock
5 signal and said status signal.

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1 8. A method of operating clock control circuitry for
2 selectively applying a clock signal to a digital processing
3 component, said clock signal capable of being changed to a
4 plurality of operating frequencies, said method of operating said
5 clock control circuitry comprising the steps of:

6 receiving a command to change a first operating
7 frequency to a second operating frequency;

8 disabling, in response to said command, said applied
9 clock signal;

10 generating a test clock signal having said second
11 operating frequency;

12 applying said test clock signal to a power supply
13 adjustment circuit; and

14 sensing a status signal from said power supply
15 adjustment circuit indicating that a power supply level of said
16 digital processing component has been adjusted to an optimum
17 value suitable for said second operating frequency.

1 9. The method of operating clock control circuitry for
2 selectively applying a clock signal to a digital processing
3 component as set forth in Claim 8 further comprising the step of
4 setting, in response to said status signal, said applied clock
5 signal to said second operating frequency.

1 10. The method of operating clock control circuitry for
2 selectively applying a clock signal to a digital processing
3 component as set forth in Claim 9 further comprising the step of
4 enabling said applied clock signal.

1 11. The method of operating clock control circuitry for
2 selectively applying a clock signal to a digital processing
3 component as set forth in Claim 8 wherein said clock control
4 circuitry comprises clock divider circuitry and a controller.

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12. A digital circuit comprising:

a digital processing component capable of operating at different clock frequencies;

an adjustable power supply capable of supplying a variable power supply level, VDD, to said digital processing component;

power supply adjustment circuitry capable of adjusting VDD; and

clock control circuitry for selectively applying a clock signal to said digital processing component, said clock signal capable of being changed to a plurality of operating frequencies, said clock control circuitry operable to (i) receive a command to change a first operating frequency to a second operating frequency, (ii) in response to said command, disable said applied clock signal, (iii) generate a test clock signal having said second operating frequency, (iv) apply said test clock signal to said power supply adjustment circuit, and (v) sense a status signal from said power supply adjustment circuit indicating that a power supply level of said digital processing component has been adjusted to an optimum value suitable for said second operating frequency.

1 13. The digital circuit as set forth in Claim 12 wherein
2 said clock control circuitry is further operable in response to
3 said status signal to set said applied clock signal to said
4 second operating frequency.

1 14. The digital circuit as set forth in Claim 13 wherein
2 said clock control circuitry is further operable to enable said
3 applied clock signal.

1 15. The digital circuit as set forth in Claim 12 wherein
2 said clock control circuitry further comprises clock divider
3 circuitry and a controller.

1 16. The digital circuit as set forth in Claim 15 wherein
2 said controller is operable to disable said applied clock signal
3 in response to said received command and enable said applied
4 clock signal in response to said status signal.

1 17. The digital circuit as set forth in Claim 15 wherein
2 said clock divider circuitry is operable to generate said test
3 clock signal having said second operating frequency.

1 18. The digital circuit as set forth in Claim 12 wherein
2 said clock control circuitry is further operable to set said
3 applied clock signal to said second operating frequency as a
4 function of said test clock signal and said status signal.

1 19. The digital circuit as set forth in Claim 12 further
2 comprising N delay cells coupled in series, each of said N delay
3 cells having a delay D determined by a value of VDD, such that a
4 clock edge applied to an input of a first delay cell ripples
5 sequentially through said N delay cells.

1 20. The digital circuit as set forth in Claim 19 wherein
2 said power supply adjustment circuitry is operable to (i) monitor
3 outputs of at least a K delay cell and a K+1 delay cell, (ii)
4 determine that said clock edge has reached an output of said K
5 delay cell and has not reached an output of said K+1 delay cell,
6 and (iii) generate a control signal capable of adjusting VDD.

1 21. The digital circuit as set forth in Claim 20 wherein
2 said power supply adjustment circuitry is further operable to
3 determine that said clock edge has reached said K delay cell
4 output and has not reached said K+1 delay cell output when a next
5 sequential clock edge is applied to said first delay cell input.

1 22. The digital circuit as set forth in Claim 21 wherein a
2 total delay from said first delay cell input to said K delay cell
3 output is greater than a maximum delay of said digital processing
4 component.